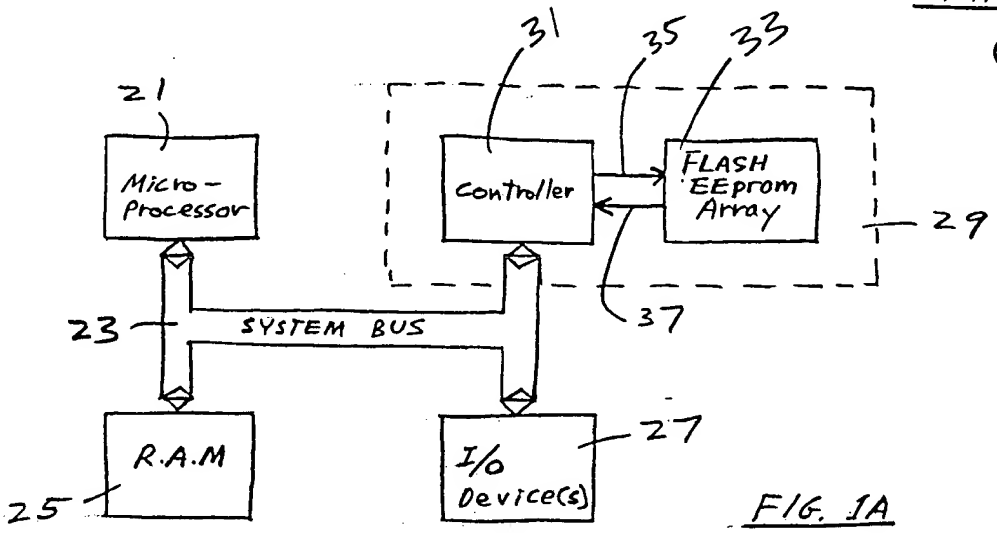

21
Micro-Processor
31
Controller
35
33
FLASH EEprom Array
29
37
23
SYSTEM BUS
R.A.M
25
I/O Device(s)
27

FIG. 1A

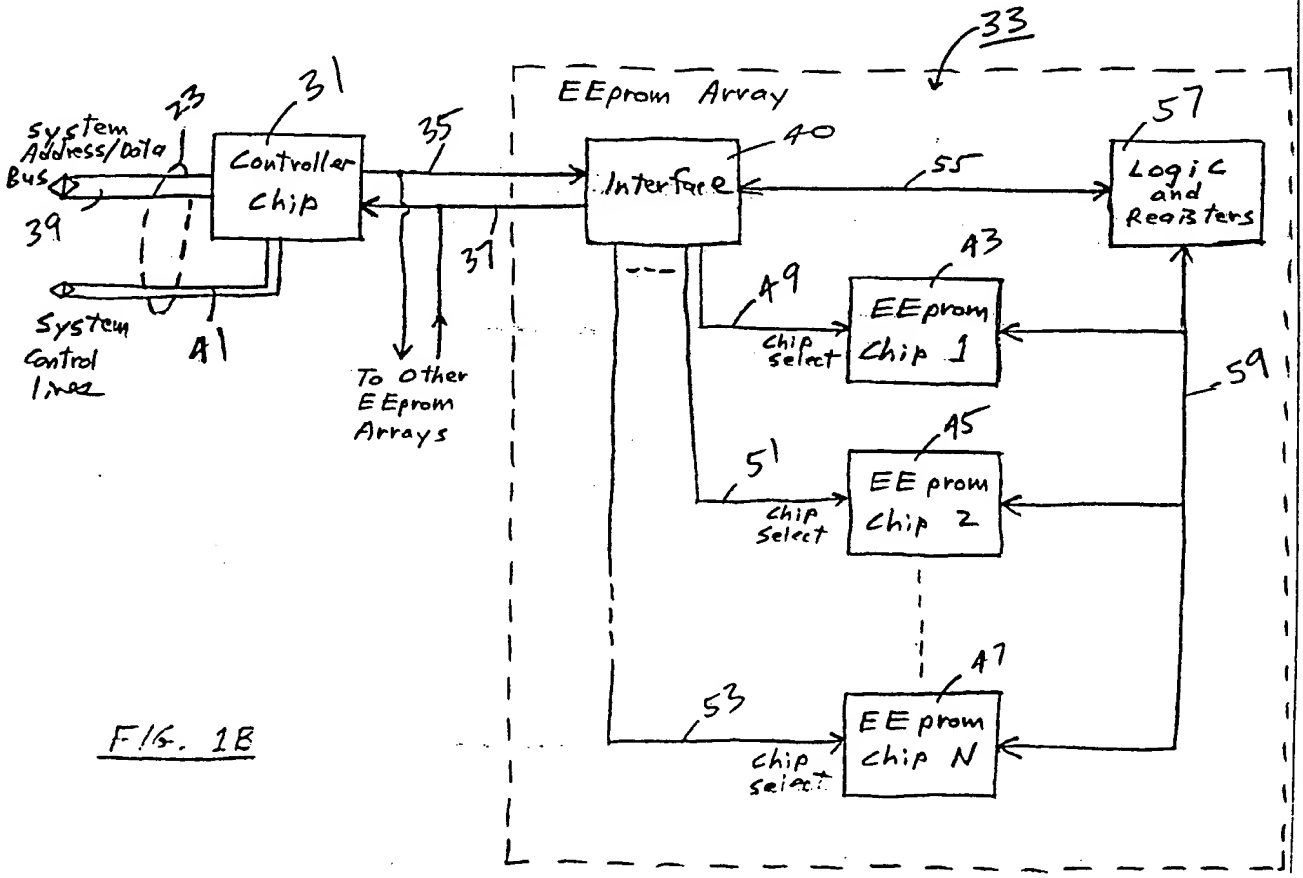

33
EEprom Array
System Address/Data Bus
23
39
31
Controller chip
35
40
Interface
55
57
Logic and Registers
System Control lines
41
37
To Other EEprom Arrays
43
49
chip select
EEprom Chip 1
59
45
51
chip select
EEprom Chip 2
47
53
chip select
EEprom chip N

FIG. 1B

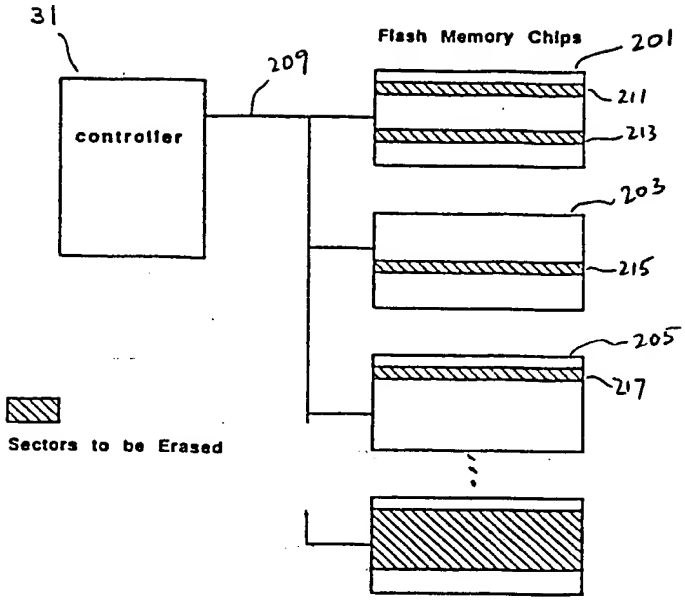


FIG_2

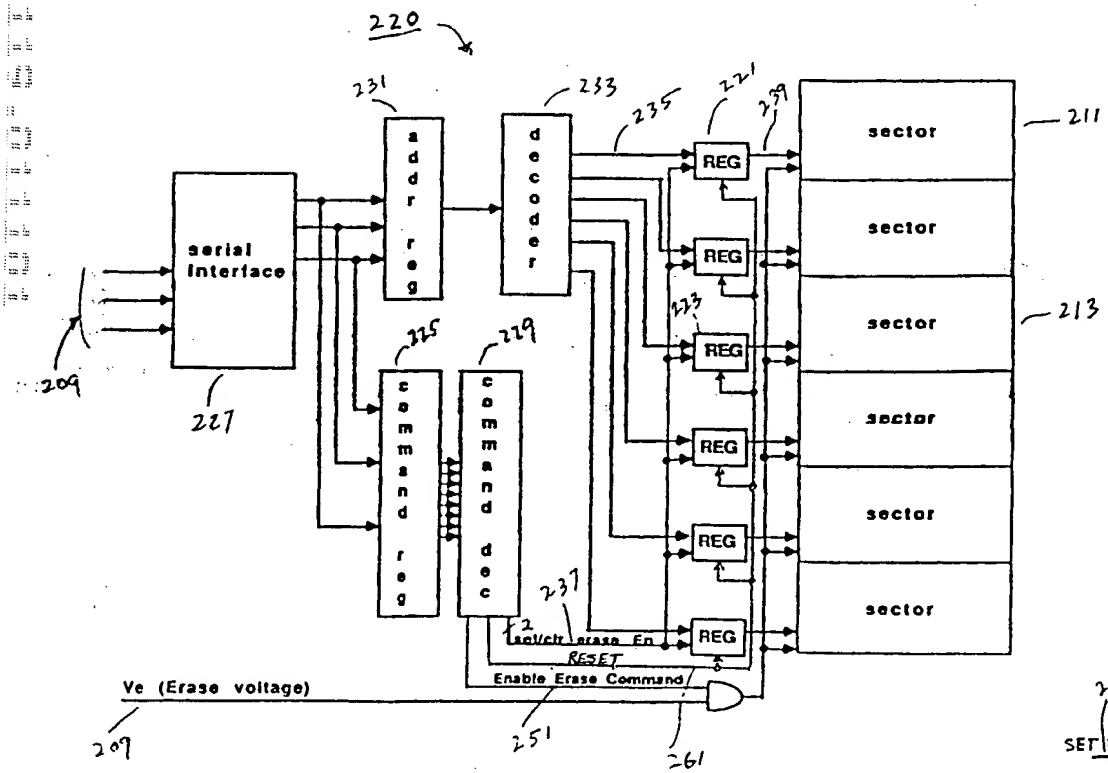


FIG_3A

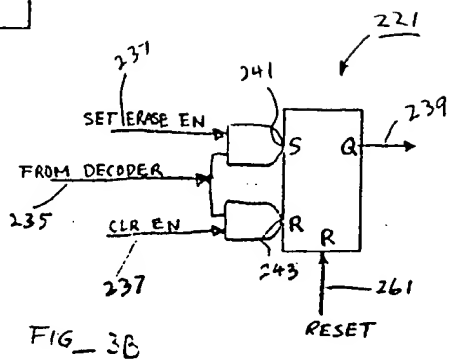


FIG_3B

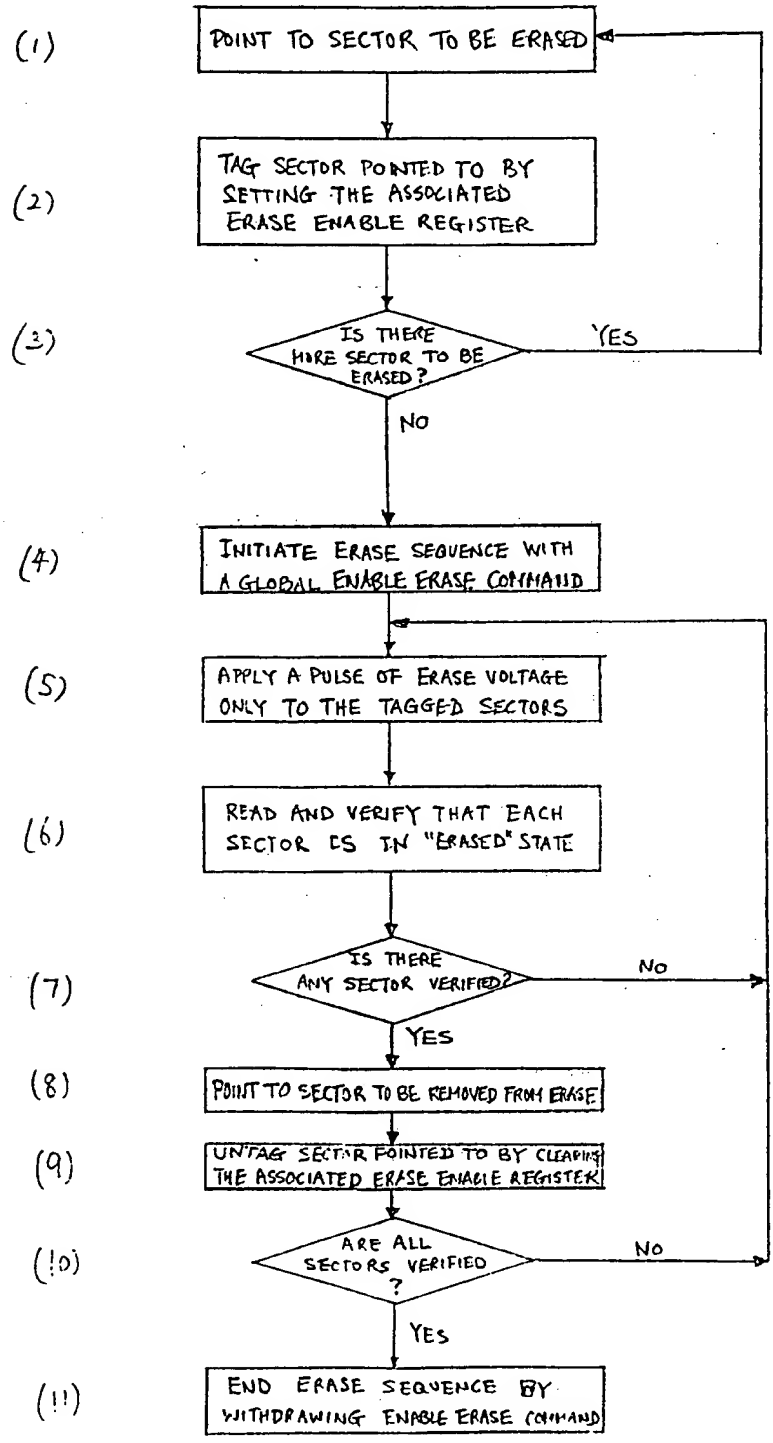
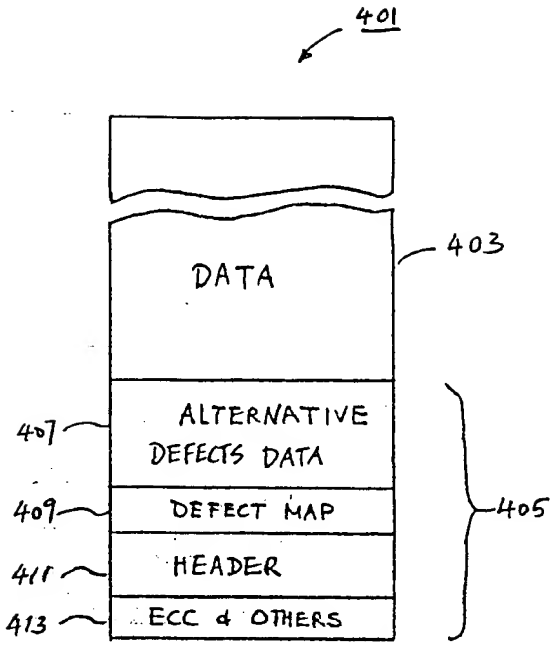
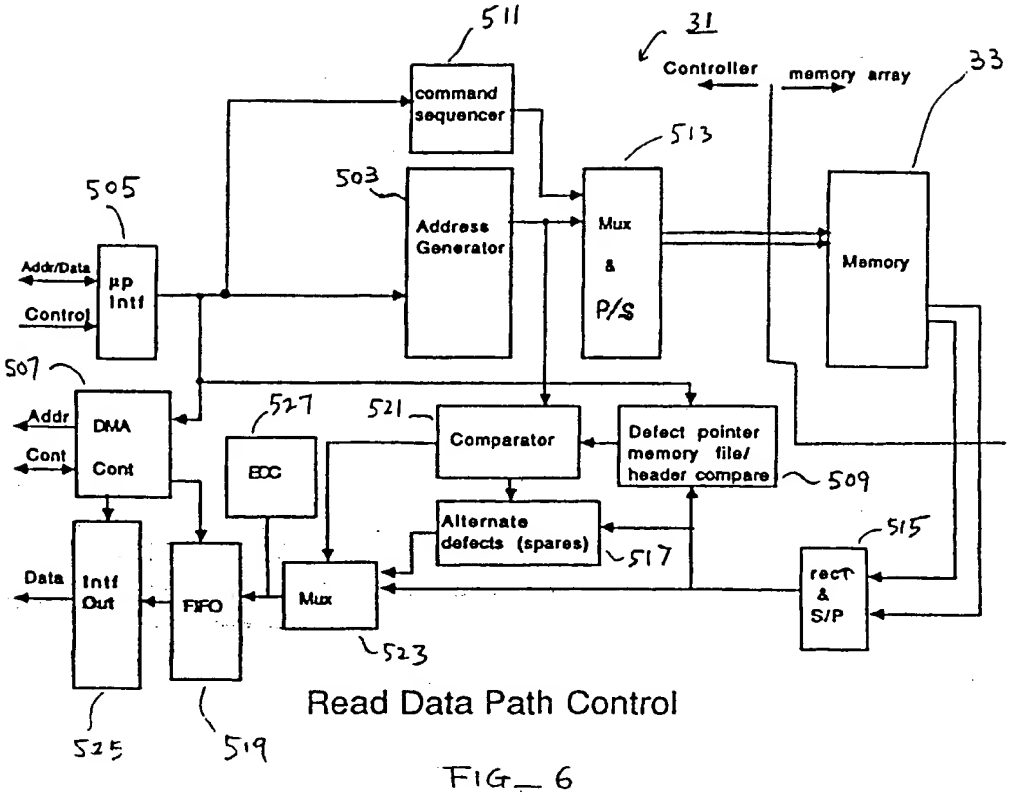

(1)
POINT TO SECTOR TO BE ERASED
(2)
TAG SECTOR POINTED TO BY SETTING THE ASSOCIATED ERASE ENABLE REGISTER
(3)
IS THERE MORE SECTOR TO BE ERASED?
YES
NO
(4)
INITIATE ERASE SEQUENCE WITH A GLOBAL ENABLE ERASE COMMAND
(5)
APPLY A PULSE OF ERASE VOLTAGE ONLY TO THE TAGGED SECTORS
(6)
READ AND VERIFY THAT EACH SECTOR IS IN "ERASED" STATE
(7)
IS THERE ANY SECTOR VERIFIED?
No
YES
(8)
POINT TO SECTOR TO BE REMOVED FROM ERASE
(9)
UNTAG SECTOR POINTED TO BY CLEARING THE ASSOCIATED ERASE ENABLE REGISTER
(10)
ARE ALL SECTORS VERIFIED ?
No
YES
(11)
END ERASE SEQUENCE BY WITHDRAWING ENABLE ERASE COMMAND

FIG_4



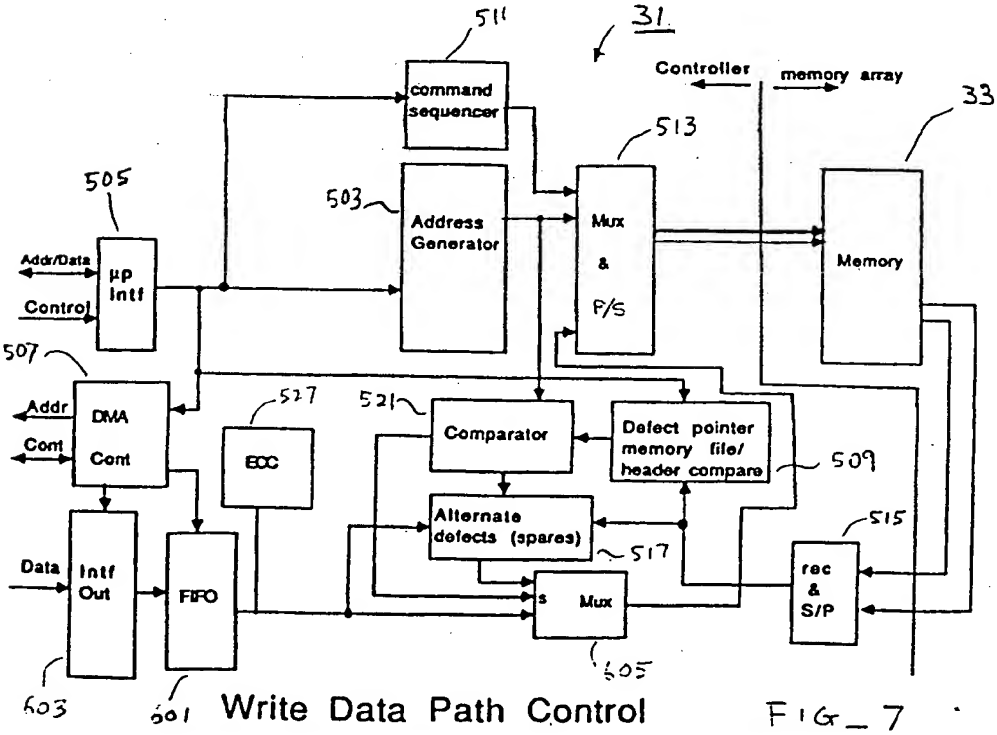
SECTOR PARTITION

FIG_5



Read Data Path Control

FIG_ 6



Write Data Path Control

FIG_ 7

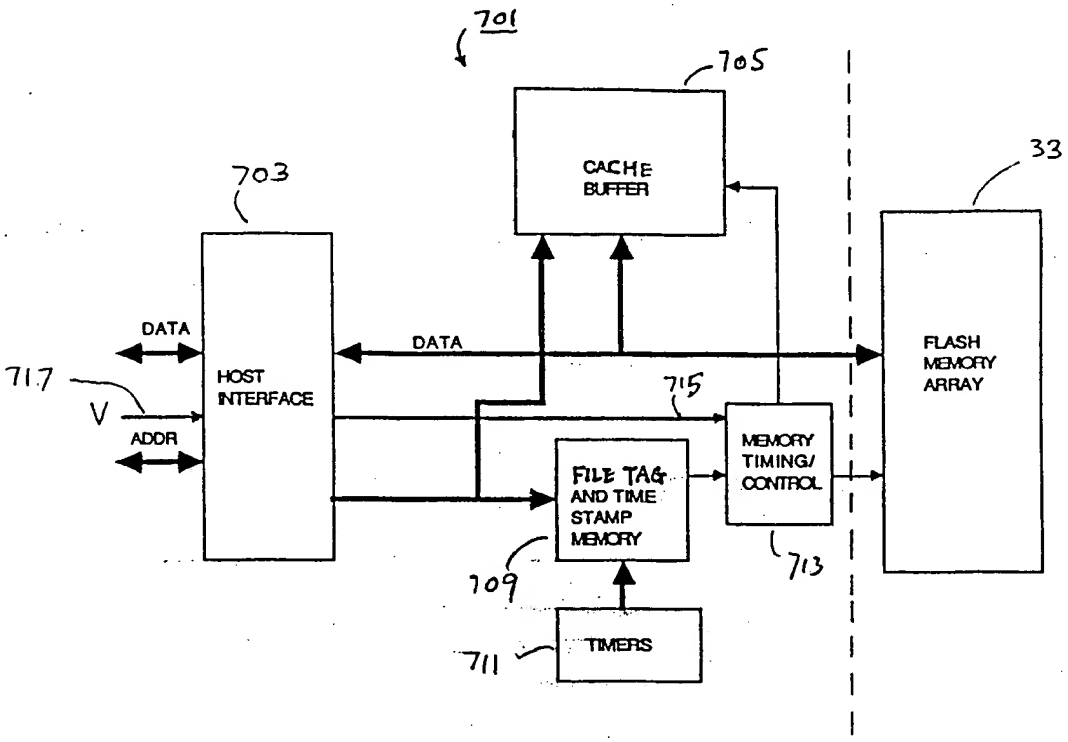

701
705
CACHE BUFFER
33
703
DATA
DATA
FLASH MEMORY ARRAY
717
V
HOST INTERFACE
715
ADDR
MEMORY TIMING/ CONTROL
FILE TAG AND TIME STAMP MEMORY
709
713
TIMERS
711

FIG_8

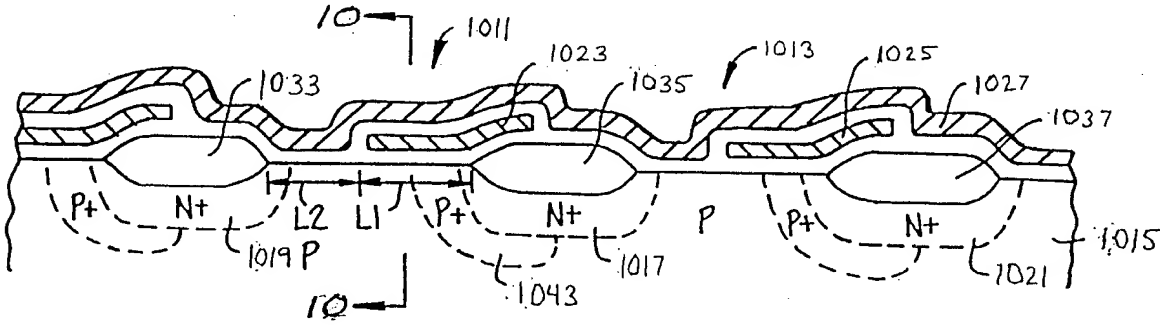


FIG. 9

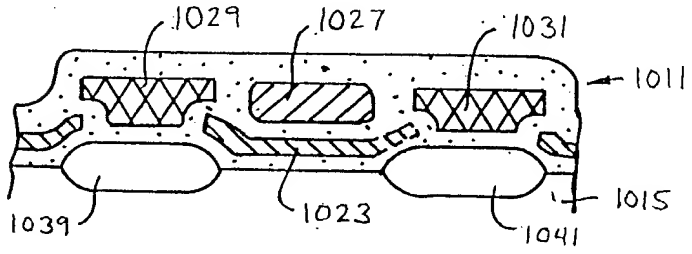


FIG. 10

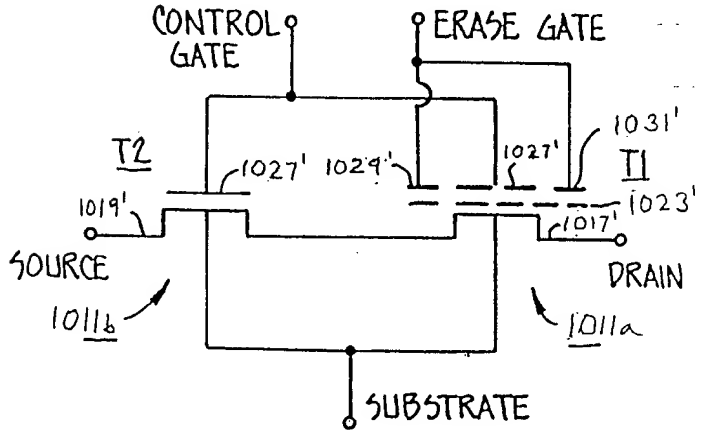


FIG. 11

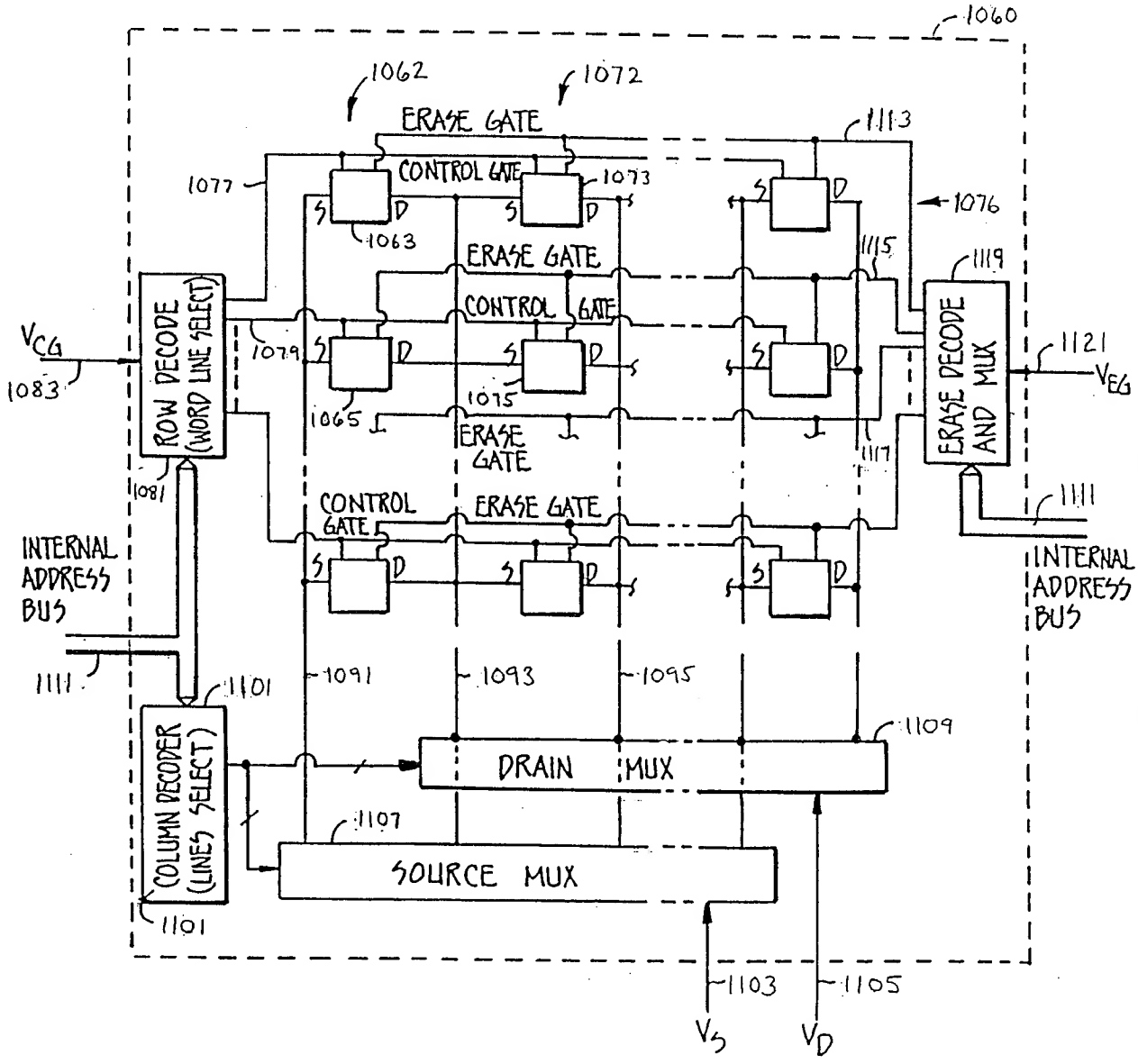

1060
1062
1072
ERASE GATE
1113
CONTROL GATE
1073
1077
1076
1063
ERASE GATE
1115
1119
CONTROL GATE
ROW DECODE (WORD LINE SELECT)
V_{CG}
1083
1079
1121
V_{EG}
1065
1075
ERASE GATE
1117
ERASE DECODE AND MUX
1081
CONTROL GATE
ERASE GATE
1111
INTERNAL ADDRESS BUS
INTERNAL ADDRESS BUS
1111
1101
1091
1093
1095
1109
DRAIN MUX
1107
SOURCE MUX
COLUMN DECODER (LINES SELECT)
1101
1103
1105
V_S
V_D

FIG. 12.

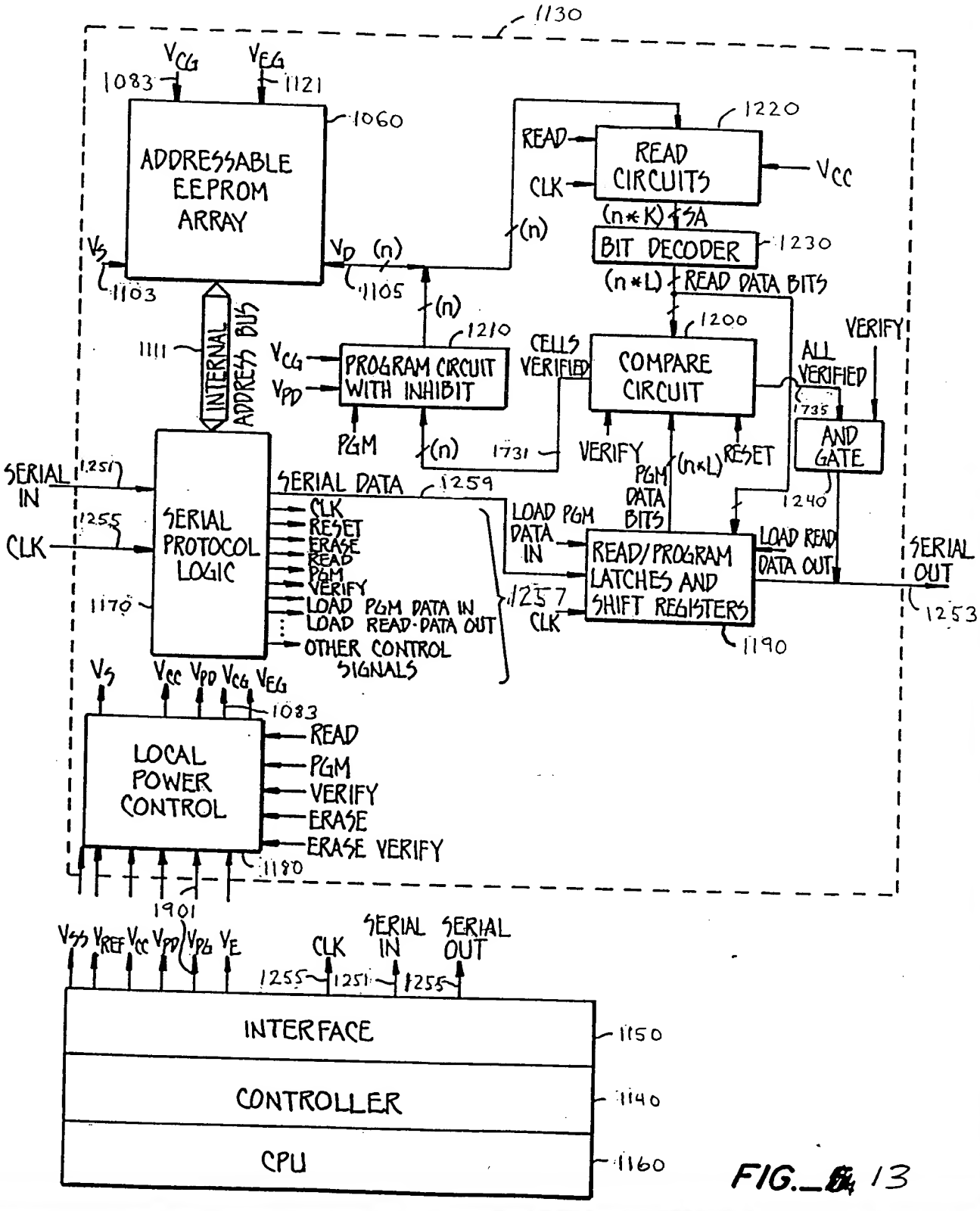

1130
V_{CG}
V_{EG}
1083
1121
ADDRESSABLE EEPROM ARRAY
1060
V_S
1103
V_D (n)
1105
INTERNAL ADDRESS BUS
1111
READ
CLK
READ CIRCUITS
1220
V_{CC}
(n*K)
SA
BIT DECODER
1230
(n*L)
READ DATA BITS
(n)
1200
COMPARE CIRCUIT
CELLS VERIFIED
ALL VERIFIED
VERIFY
1735
AND GATE
1240
V_{CG}
V_{PP}
PROGRAM CIRCUIT WITH INHIBIT
1210
PGM
(n)
1731
VERIFY
(n*L)
RESET
PGM DATA BITS
SERIAL IN
1251
CLK
1255
SERIAL PROTOCOL LOGIC
1170
SERIAL DATA
1259
CLK
RESET
ERASE
READ
PGM
VERIFY
LOAD PGM DATA IN
LOAD READ DATA OUT
OTHER CONTROL SIGNALS
LOAD PGM DATA IN
1257
CLK
READ/PROGRAM LATCHES AND SHIFT REGISTERS
1190
LOAD READ DATA OUT
SERIAL OUT
1253
V_S
V_{CC}
V_{PD}
V_{CG}
V_{EG}
1083
LOCAL POWER CONTROL
READ
PGM
VERIFY
ERASE
ERASE VERIFY
1180
1901
V_{SS}
V_{REF}
V_{CC}
V_{PD}
V_{PG}
V_E
CLK
SERIAL IN
SERIAL OUT
1255
1251
1255
INTERFACE
1150
CONTROLLER
1140
CPU
1160

FIG. 13

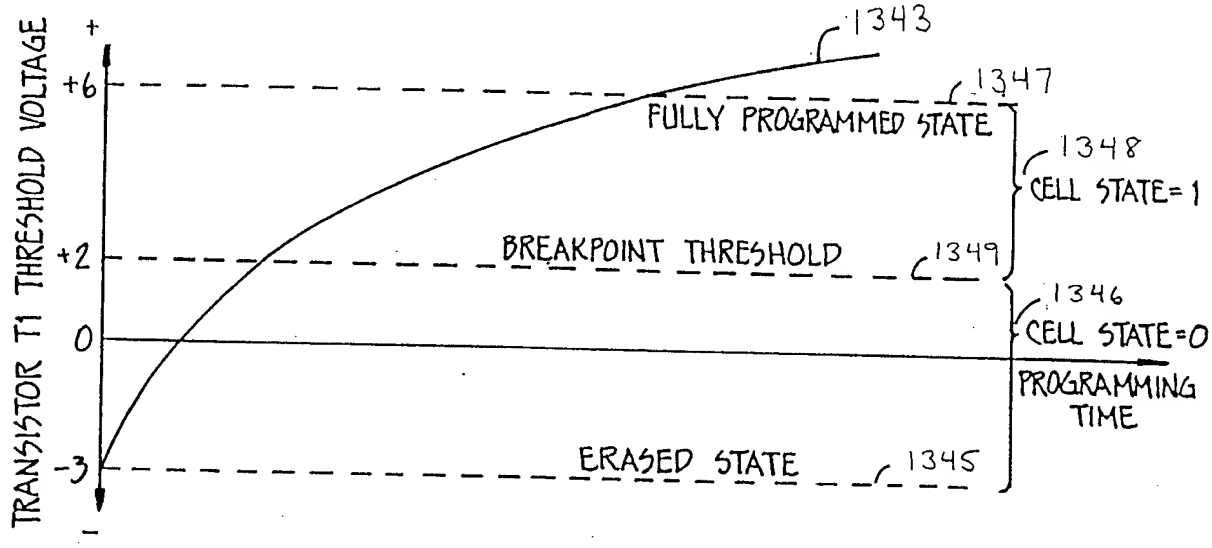


FIG. 14.

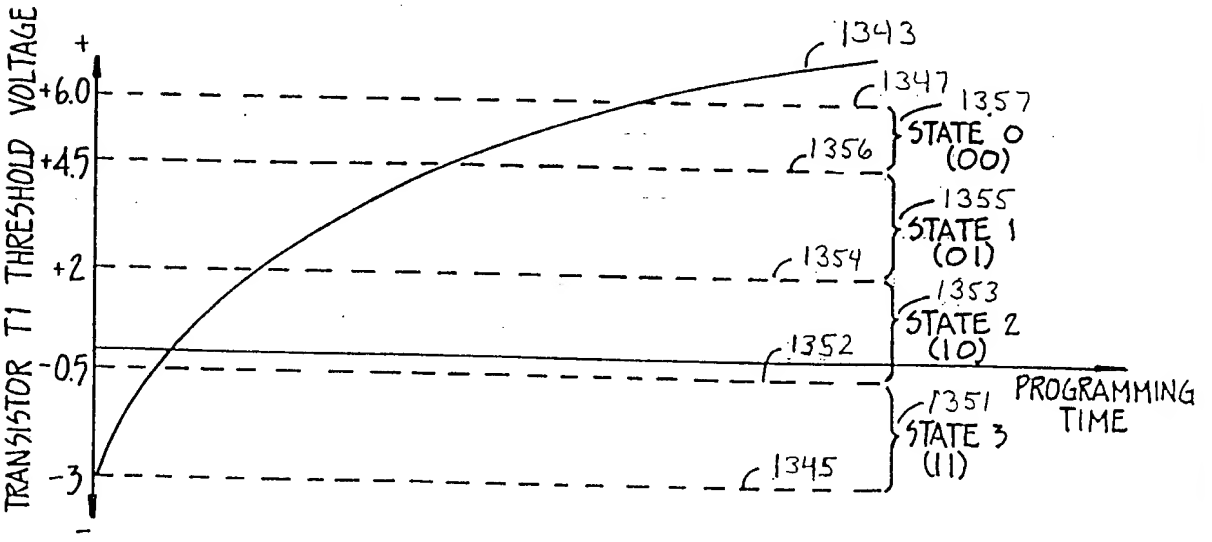


FIG. 15A

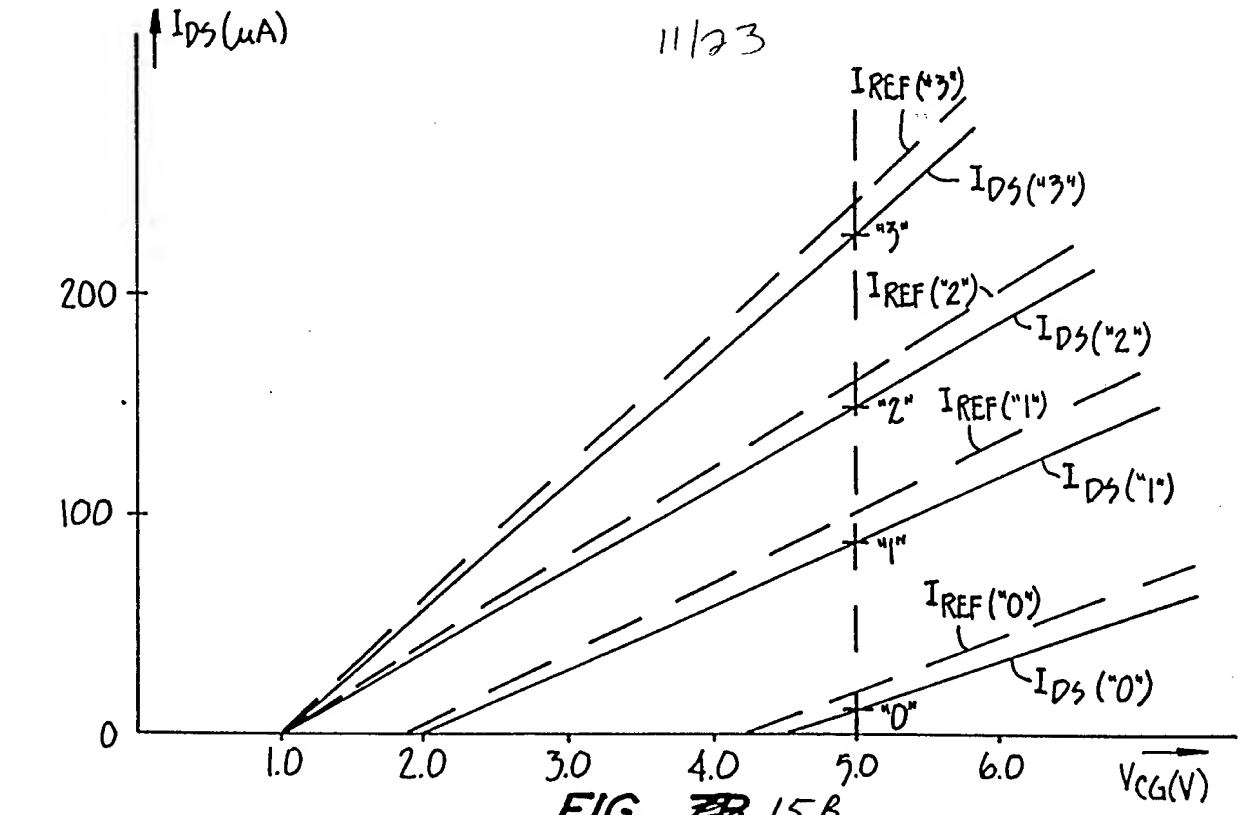


FIG. ~~7B~~ 15B

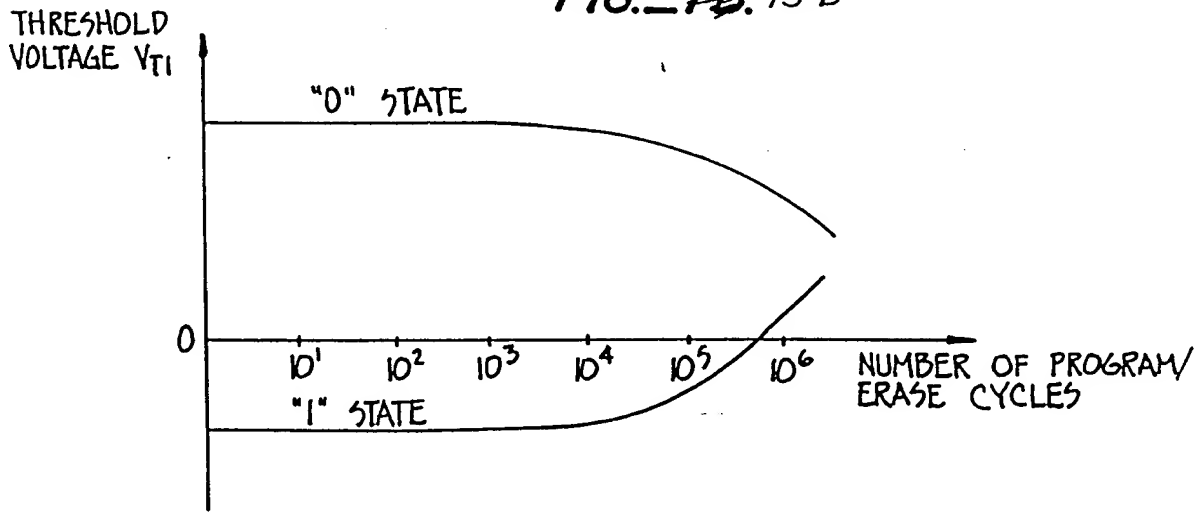


FIG. ~~8A~~ 16A

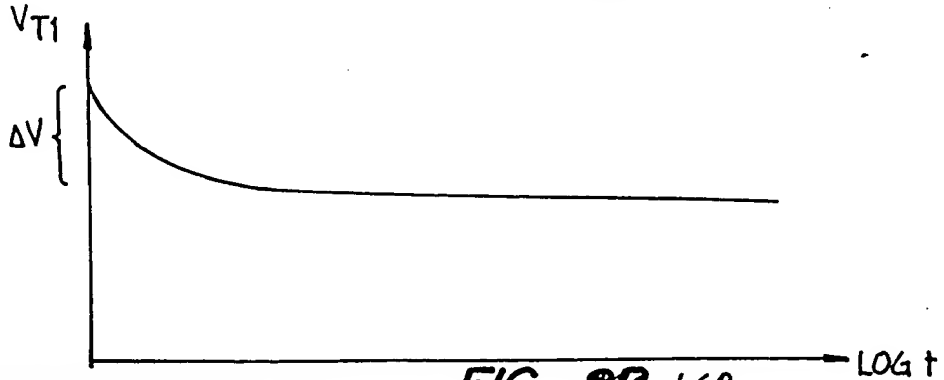


FIG. ~~8B~~ 16B

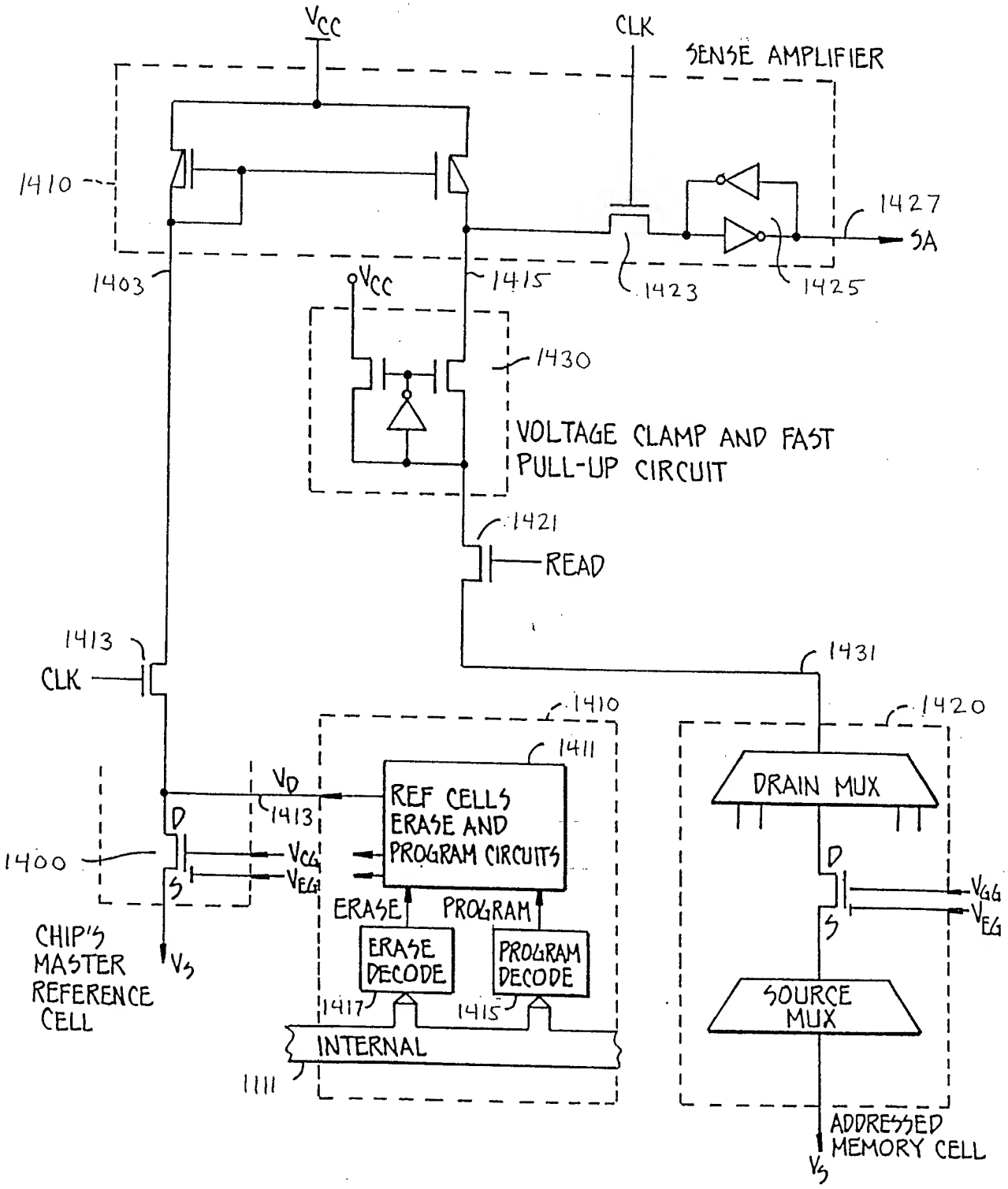

V_{CC}
CLK
SENSE AMPLIFIER
1410
1427
SA
1403
1415
1423
1425
V_{CC}
1430
VOLTAGE CLAMP AND FAST PULL-UP CIRCUIT
1421
READ
1413
CLK
1431
1410
1420
1411
V_D
1413
REF CELLS ERASE AND PROGRAM CIRCUITS
DRAIN MUX
D
1400
V_{GG}
V_{EG}
S
ERASE
PROGRAM
ERASE DECODE
PROGRAM DECODE
CHIP'S MASTER REFERENCE CELL
V_S
1417
1415
INTERNAL
1111
SOURCE MUX
ADDRESSED MEMORY CELL
V_S

FIG. 17A

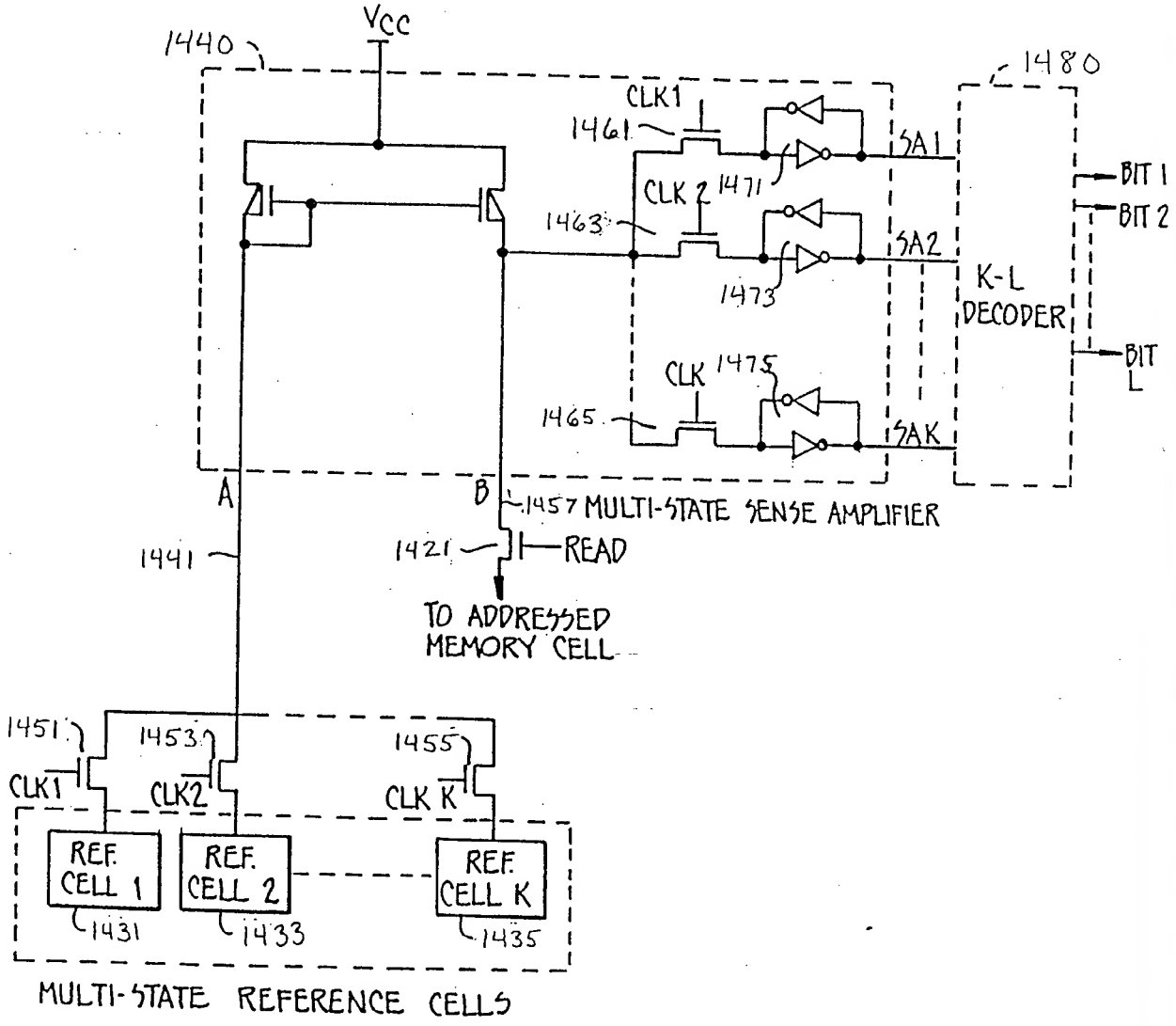

Vcc
1440
1480
CLK1
1461
SA1
1471
CLK 2
1463
SA2
1473
K-L
DECODER
BIT 1
BIT 2
BIT
L
CLK
1475
1465
SAK
A
B
1457 MULTI-STATE SENSE AMPLIFIER
1441
1421
READ
TO ADDRESSED
MEMORY CELL
1451
1453
1455
CLK1
CLK2
CLK K
REF.
CELL 1
REF.
CELL 2
REF.
CELL K
1431
1433
1435
MULTI-STATE REFERENCE CELLS

FIG. 17B

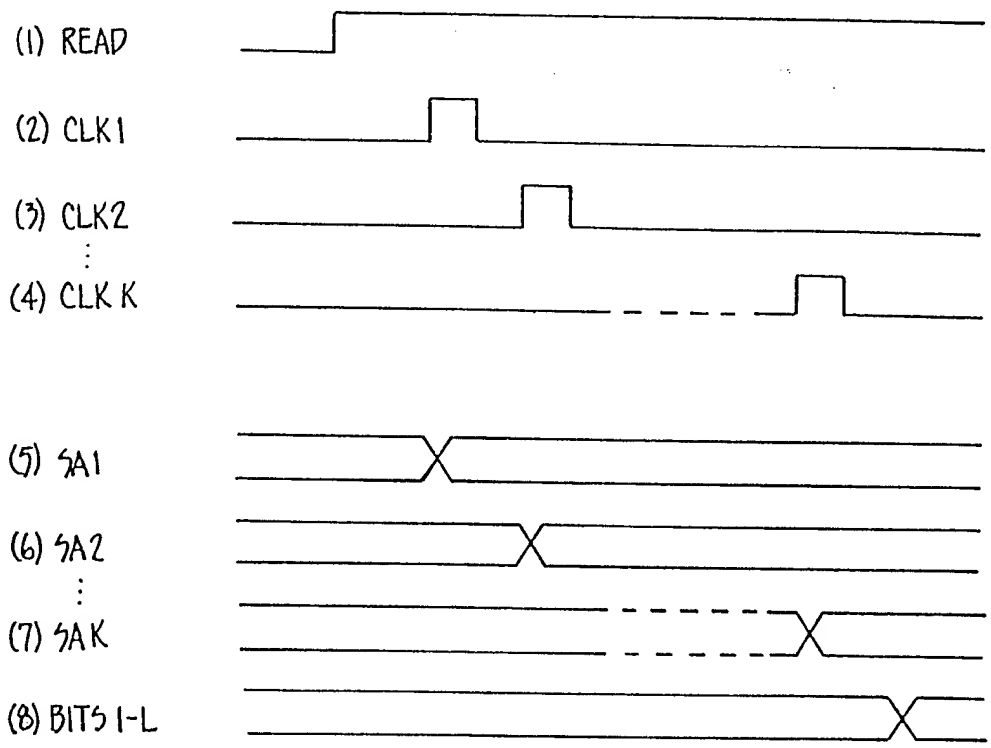


FIG. 17C

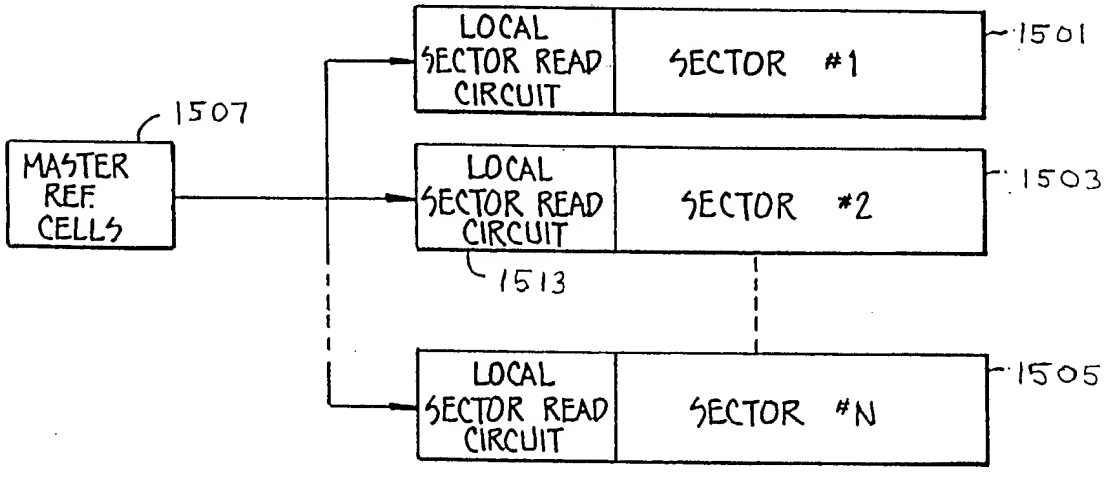


FIG. 18

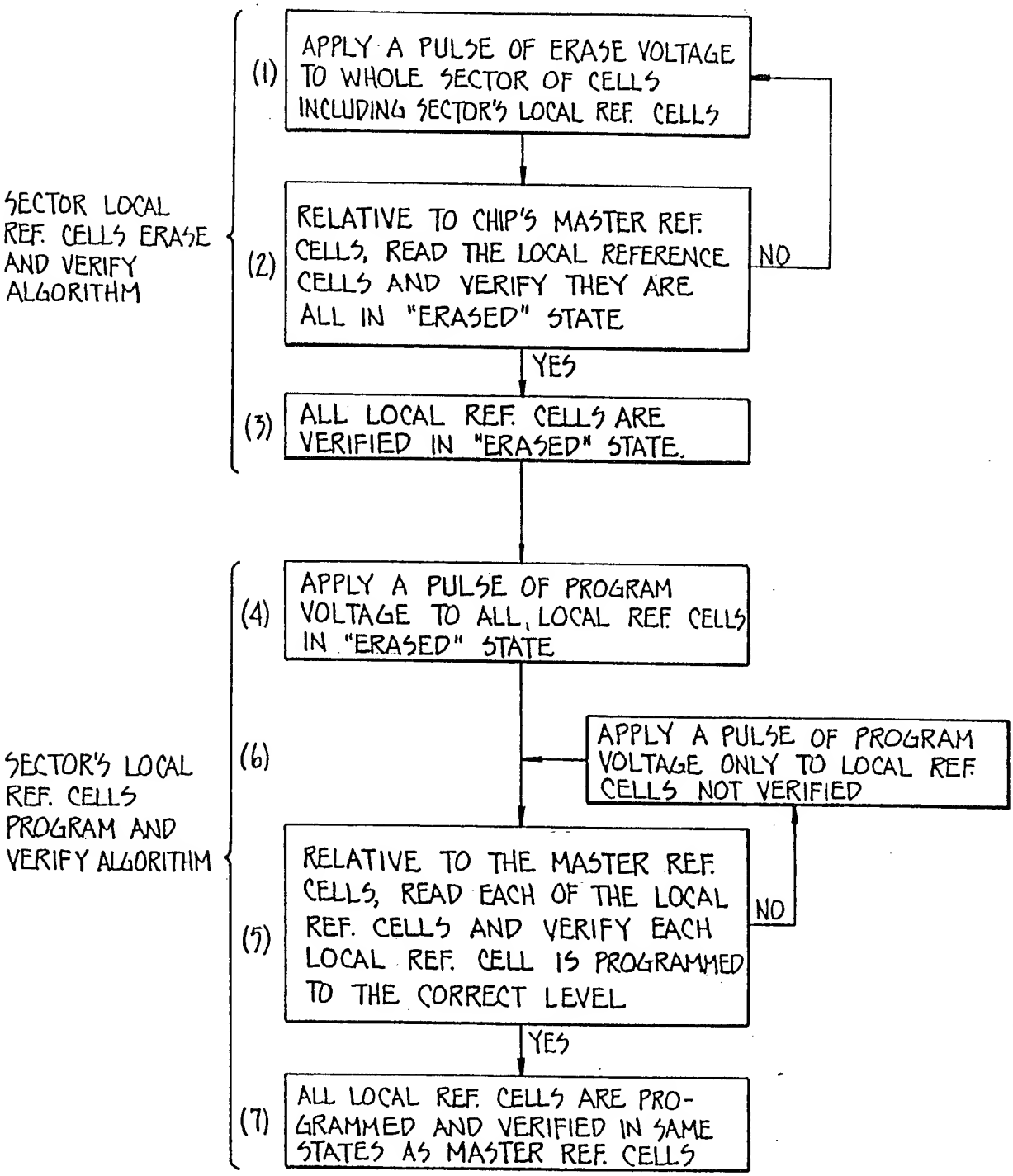

SECTOR LOCAL REF. CELLS ERASE AND VERIFY ALGORITHM
(1) APPLY A PULSE OF ERASE VOLTAGE TO WHOLE SECTOR OF CELLS INCLUDING SECTOR'S LOCAL REF. CELLS
(2) RELATIVE TO CHIP'S MASTER REF. CELLS, READ THE LOCAL REFERENCE CELLS AND VERIFY THEY ARE ALL IN "ERASED" STATE
NO
YES
(3) ALL LOCAL REF. CELLS ARE VERIFIED IN "ERASED" STATE.
SECTOR'S LOCAL REF. CELLS PROGRAM AND VERIFY ALGORITHM
(4) APPLY A PULSE OF PROGRAM VOLTAGE TO ALL LOCAL REF. CELLS IN "ERASED" STATE
(6) APPLY A PULSE OF PROGRAM VOLTAGE ONLY TO LOCAL REF. CELLS NOT VERIFIED
(5) RELATIVE TO THE MASTER REF. CELLS, READ EACH OF THE LOCAL REF. CELLS AND VERIFY EACH LOCAL REF. CELL IS PROGRAMMED TO THE CORRECT LEVEL
NO
YES
(7) ALL LOCAL REF. CELLS ARE PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS

FIG. 19

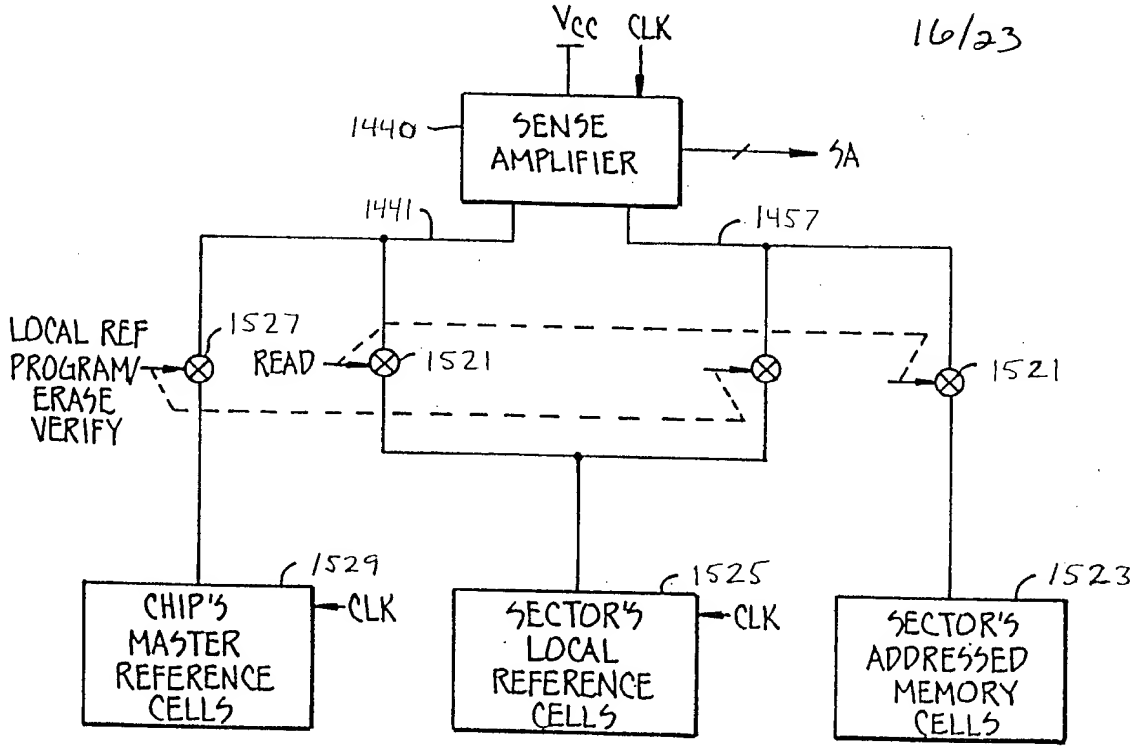


FIG. ~~12A~~ 20A

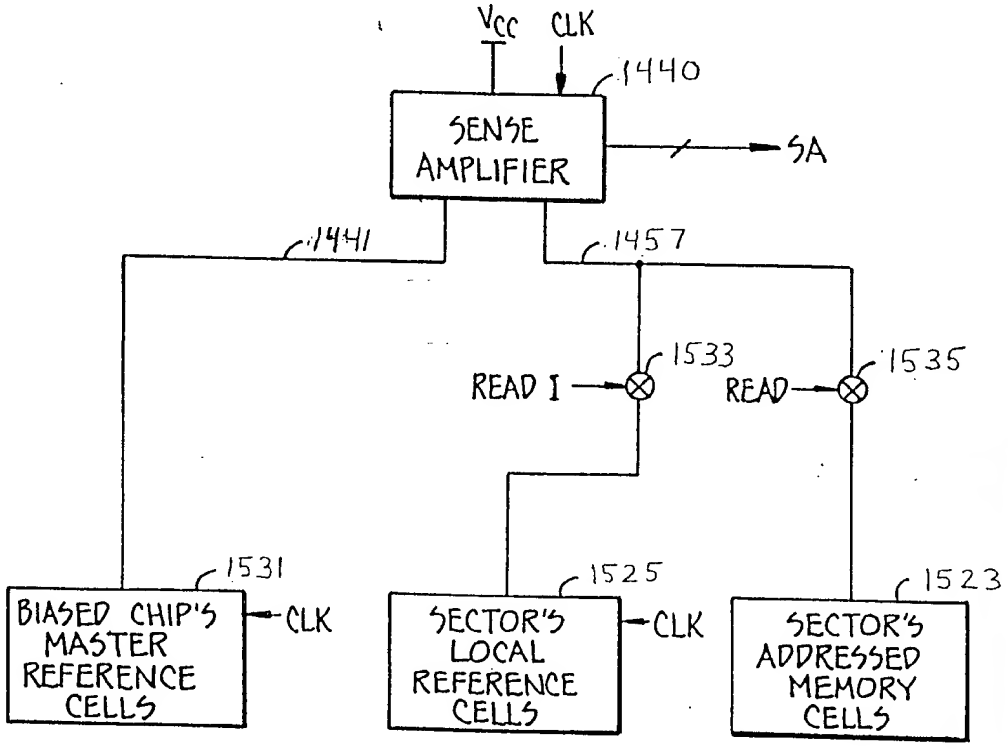


FIG. ~~13A~~ 21A

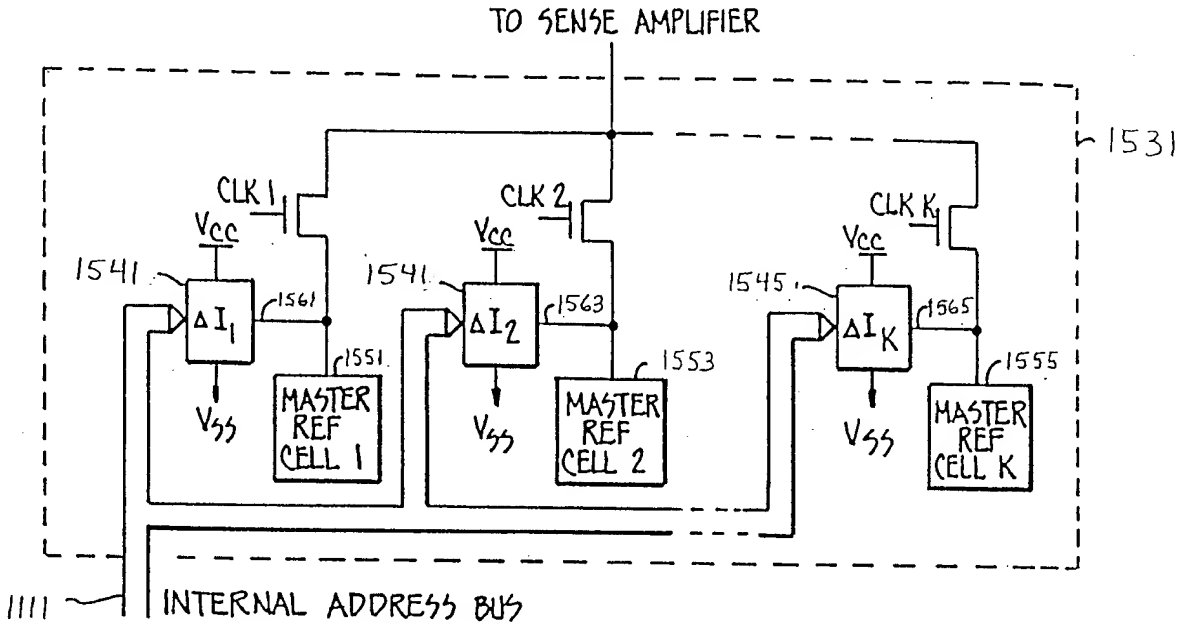


FIG. 21B

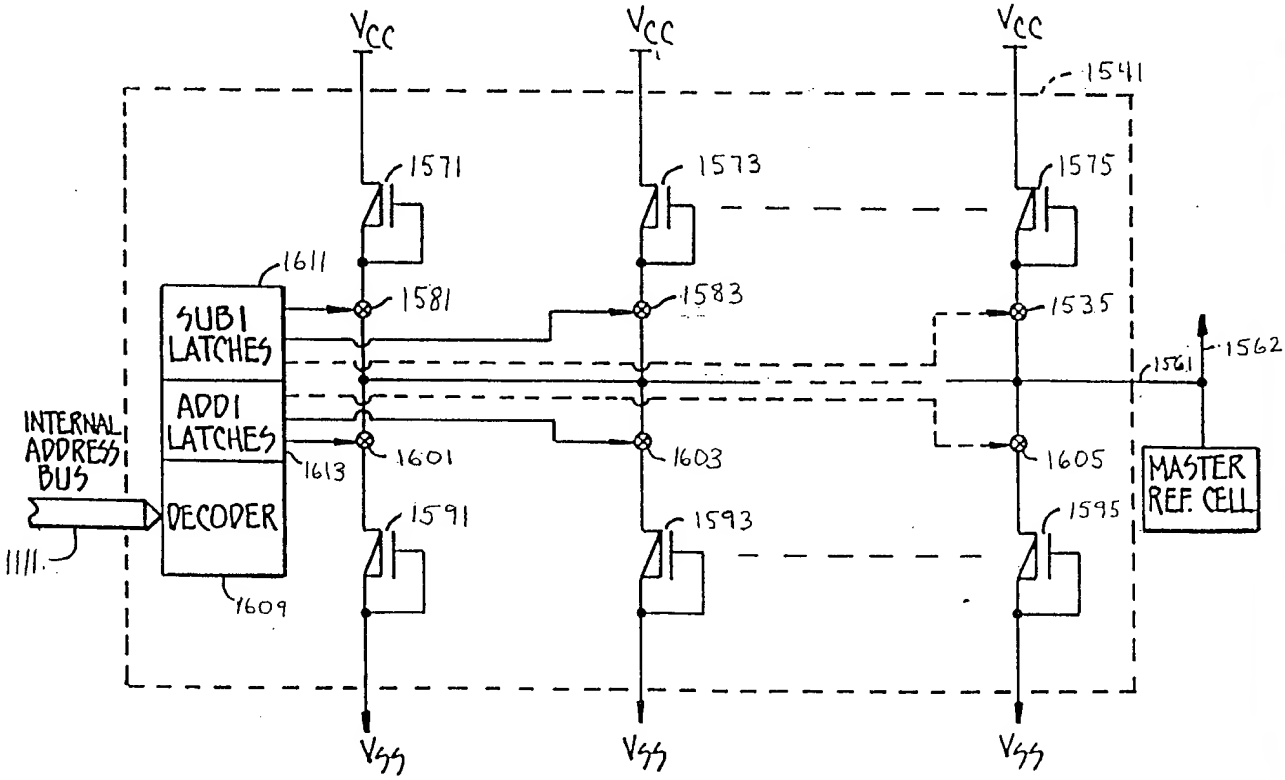


FIG. 21C

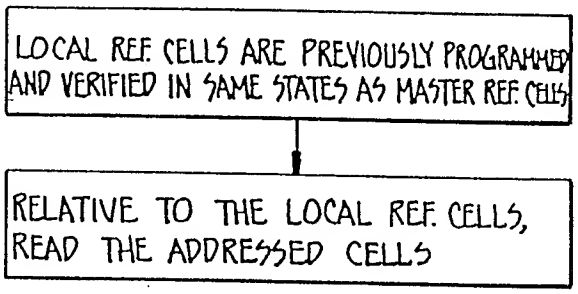


FIG. ~~12B~~, 20B

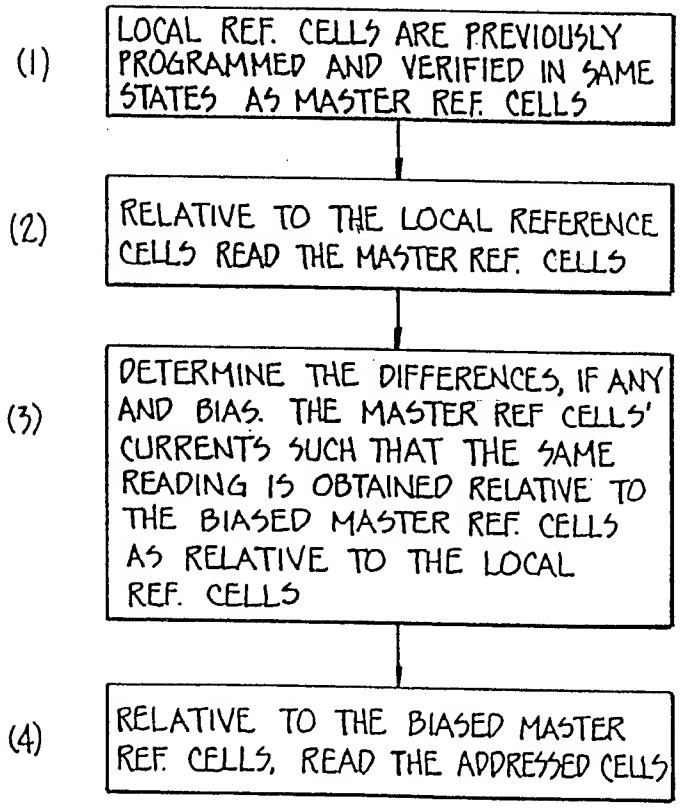
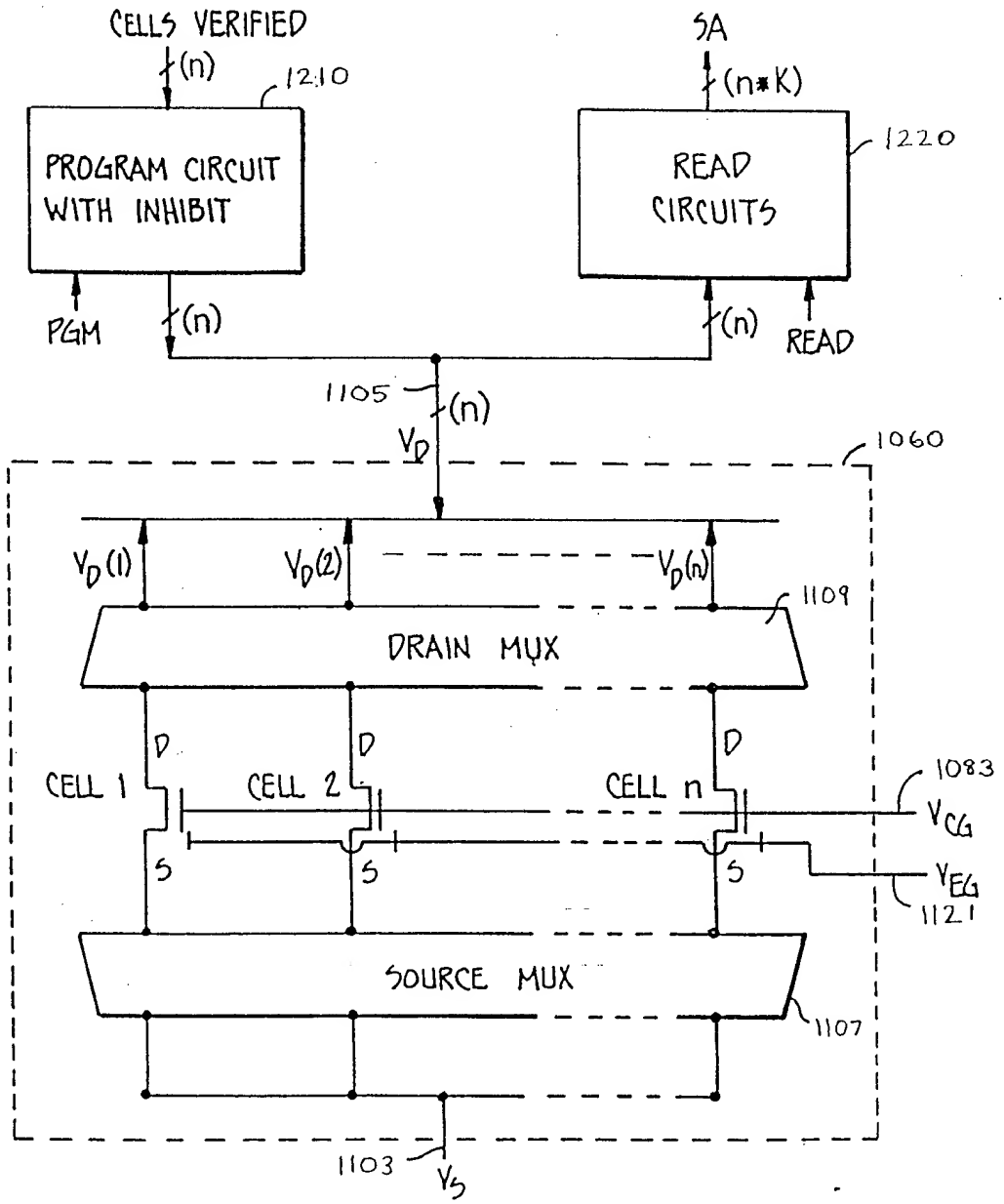
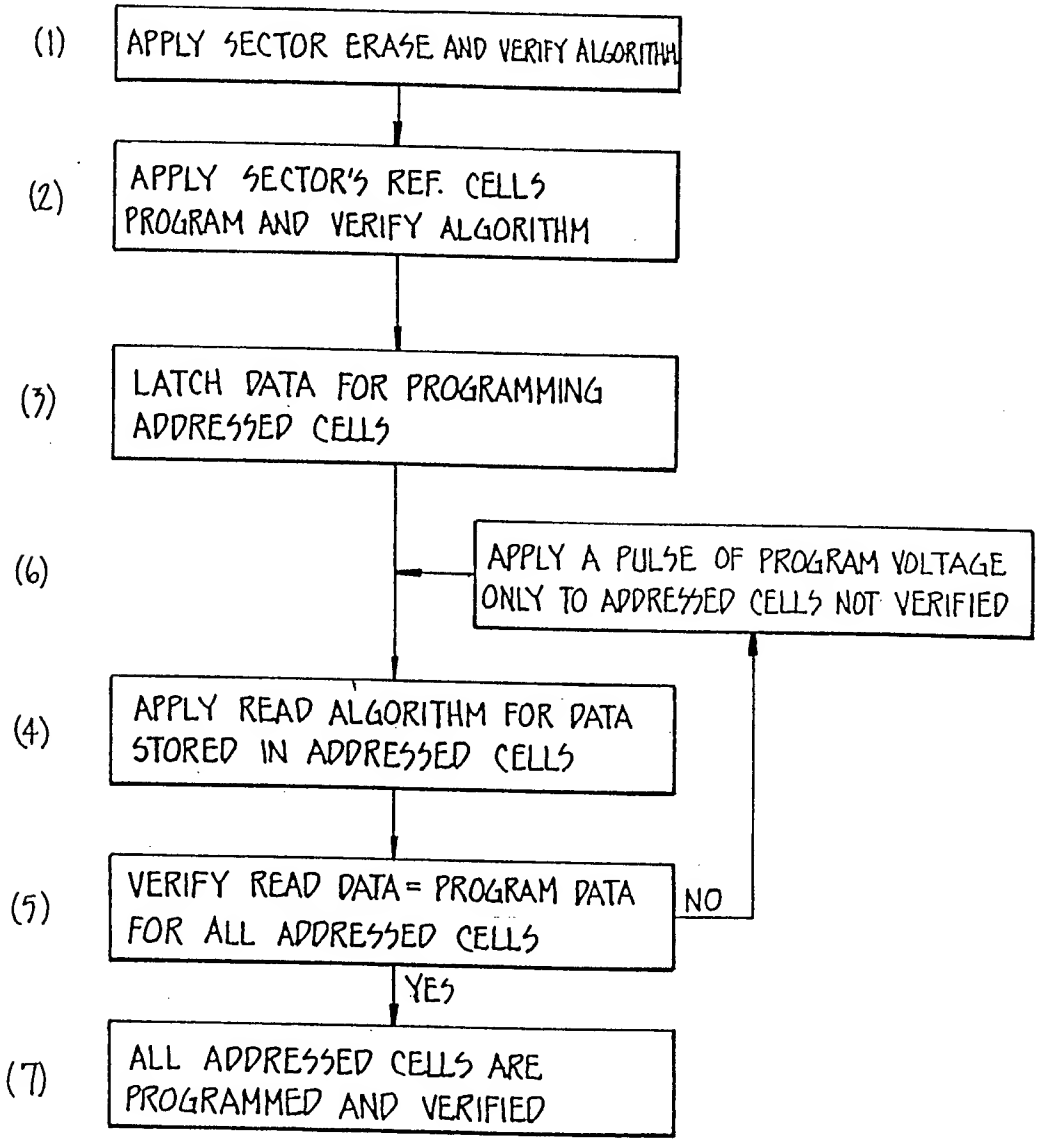


FIG. ~~12D~~, 21D



READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG. 22.



PROGRAM ALGORITHM

FIG. 15. 23

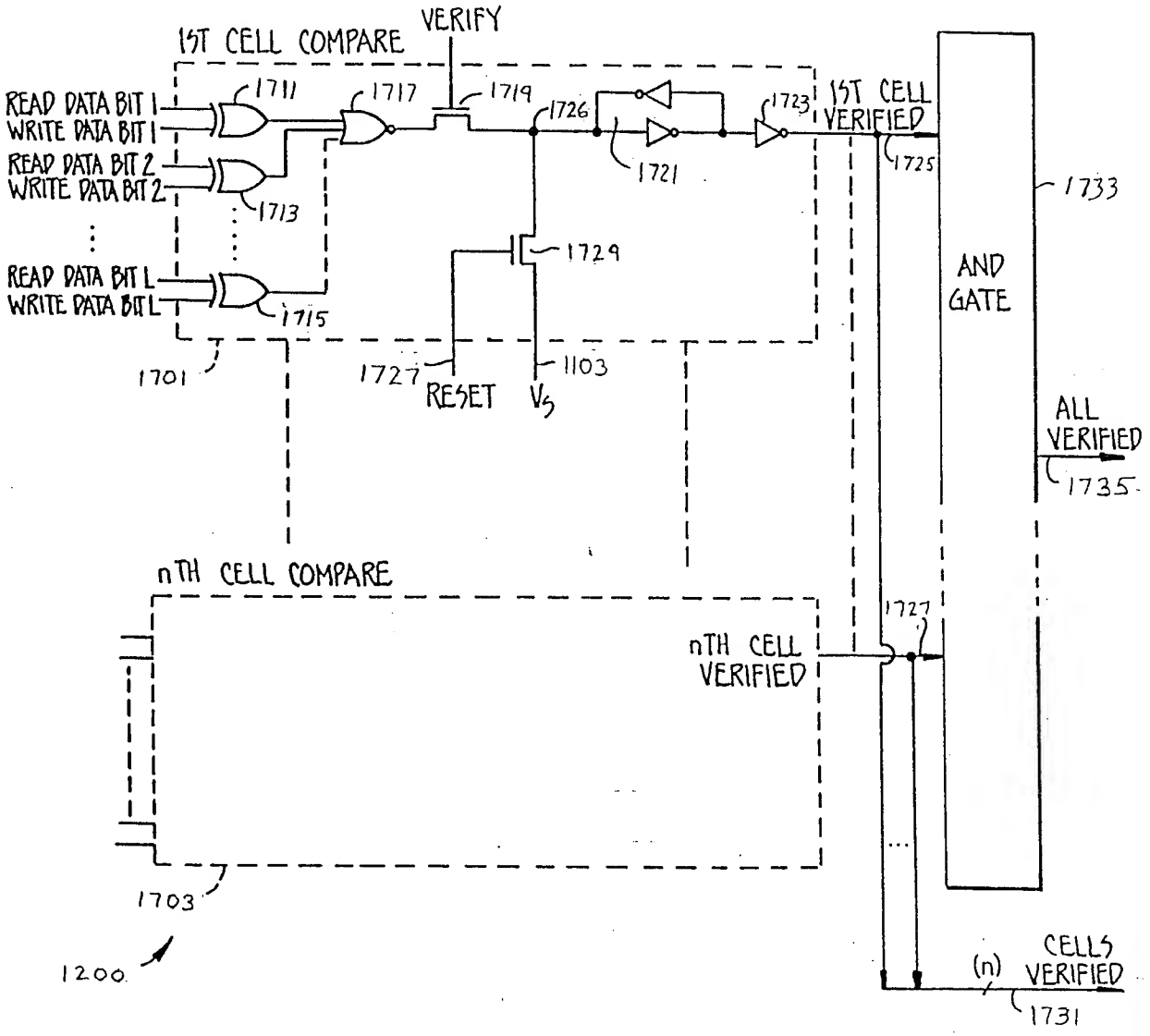

1ST CELL COMPARE
VERIFY
READ DATA BIT 1
WRITE DATA BIT 1
READ DATA BIT 2
WRITE DATA BIT 2
READ DATA BIT L
WRITE DATA BIT L
1711
1717
1719
1726
1723
1721
1725
1713
1715
1729
1727
RESET
1103
1701
1ST CELL VERIFIED
AND GATE
1733
ALL VERIFIED
1735
nTH CELL COMPARE
nTH CELL VERIFIED
1727
1703
1200
(n) CELLS VERIFIED
1731

FIG. 16. 24

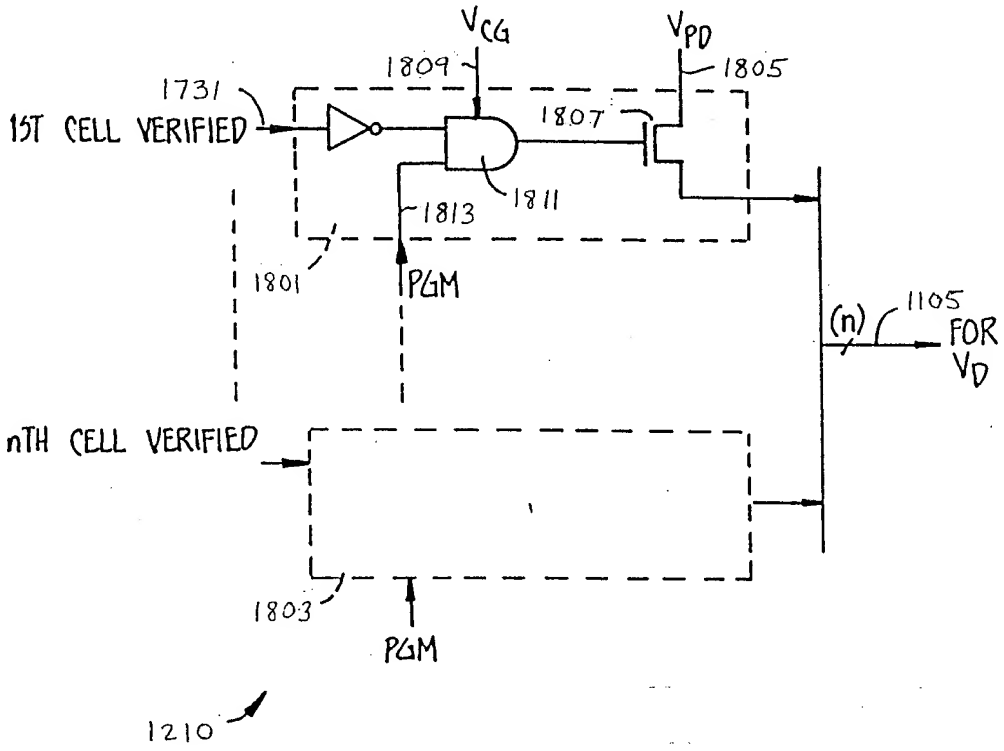

V_{CG}
V_{PD}
1809
1805
1731
1ST CELL VERIFIED
1807
1811
1813
1801
PGM
(n)
1105
FOR V_D
nTH CELL VERIFIED
1803
PGM
1210

FIG. 25

	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

~~TABLE 1~~ FIG. 26

(typical values)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12v	$V_{CC}+\delta V$	V_{CC}	$V_{CC}-\delta V$
V_{CC}	5v	5v	5v	5v	5v
V_{PD}	V_{SS}	8v	8v	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20v	V_{SS}
unselected control gate	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
unselected bit line	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

V_{SS}=0V, V_{REF}=1.5V, δV=0.5V - 1V

~~TABLE 2~~ FIG. 27